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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,092	09/08/2003	Satoshi Kitamura	SIC-03-035	2091
29863 7590 07/06/2007 DELAND LAW OFFICE P.O. BOX 69 KLAMATH RIVER, CA 96050-0069			EXAMINER PARRIES, DRU M	
			ART UNIT	PAPER NUMBER
			2836	
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			07/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/605,092

Applicant(s)

KITAMURA ET AL.

Examiner

Dru M. Parries

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 April 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 38-62 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 38-62 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 38-62 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).
4. Claims 38-48 and 57-62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Turner (2002/0014366) and Nakabayashi et al. (JP 04-150729 A). Turner teaches a bicycle power supply comprising an AC power supply (172) supplying power to a variety of electrical components (160-168; 174-184) through a plurality of batteries (170). He also teaches a rectifier (154) that converts the AC power to DC current to supply power to the plurality of storage elements. He also teaches some of the electrical components to be a mechanical adjusting

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mechanism (166, 168) (i.e. transmission or suspension), a microprocessor (150) and a sensor element (184) where the mechanical adjusting mechanism has a higher capacitance than the microprocessor. Turner fails to teach separate storage elements providing power to separate electrical components and a unit that prevents power flow from one storage element to another. Nakabayashi teaches two different storage elements (1st - 7 and 2nd - 12, 13) in parallel each structured to supply power to its own electrical component (10 and 16). He also teaches a power-inhibiting unit (11) to prevent power flow from the first storage element to the second component and from the second storage element to the first component. He also teaches reverse current inhibiting unit (15) coupled between the first and second storage elements to inhibit flow from the second storage element to the first. He also teaches preserving power in the first storage element when current is drawn from the second storage element to the second voltage system (16). He also teaches that current flows from the first storage element to the second via the reverse current inhibiting unit. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the plurality of batteries to supply power to their own individual loads (i.e. the first storage element supplying power to the mechanical adjusting mechanism and the second storage element supplying power to the microprocessor and/or a sensor element) to be able to supply precise output values to each component in the system thereby creating a more efficient system and eliminating the possibility of voltage fluctuation due to other loads and/or storage elements. It also would have been obvious to one of ordinary skill in the art at the time of the invention to use the power and reverse current inhibiting units to eliminate stray currents that may cause malfunction in the system. None of the references explicitly teach which storage elements supply power to which electrical component, however, it

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would be obvious to pair any particular electrical component with any particular storage element since it has been held that rearranging parts (i.e. storage elements to corresponding electrical components) of an invention involves only routine skill in the art. *In re Japikse*, 86 USPQ 70.

5. Claims 49-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Turner (2002/0014366) and Nakabayashi et al. (JP 04-150729 A) as applied to claims 38, 39, 43, and 48 above, and further in view of Mitchell (6,355,990) and Winick et al. (2002/0135235). Turner and Nakabayashi teach a bicycle power supply system as described above. Nakabayashi also teaches a second diode. Turner fails to explicitly teach a) the storage elements being in parallel, b) a method to inhibit current to flow from the first storage element toward the AC power supply, c) a power switch unit, and d) a method of supplying power to the storage elements. Mitchell teaches a) a power distribution system with a plurality of parallel storage elements (C1, C2, C3). He also teaches d) selectively switching current from a power supply to each storage element (via switches S1, S2, S3) in response to a voltage at each storage element. Winick teaches b) & c) a power switch unit (174) comprising a first diode that prevents current anywhere in the circuit from flowing toward a power supply (114) (Abstract; [0037]). It would have been obvious to one of ordinary skill in the art at the time of the invention to place Turner's storage elements in parallel since Mitchell teaches a parallel storage system known to work in the art and Turner was silent as to the configuration of the storage elements. It also would have been obvious to one of ordinary skill in the art at the time of the invention to implement Mitchell's method of charging the storage elements so that each storage element will have the correct amount of stored voltage to power each individual load. It also would have been obvious to one of ordinary skill in the art

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at the time of the invention to implement Winick's power switch unit into Turner's invention so that current can be prohibited from flowing to the AC power supply and cause a malfunction.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dru M. Parries whose telephone number is (571) 272-8542. The examiner can normally be reached on Monday -Thursday from 9:00am to 6:00pm. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry, can be reached on 571-272-2800 x 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMP

6-22-2007



MICHAEL SHERRY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800